GLOBAL INITIATIVE FOR ACADEMIC NETWORKS

Ministry of Human Resource Development
Government of India

सत्यमेव जयते

GLOBAL INITIATIVE FOR ACADEMIC NETWORKS

National Coordinating Institute
INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

www.gian.iitkgp.ac.in

VLSI ARCHITECTURES FOR SIGNAL PROCESSING AND MACHINE LEARNING

Overview

This course brings together the distinct fields of computer architecture, VLSI, digital signal processing, and machine learning. Digital signal processing is an enabling technology for many applications such as video, speech, wired and wireless communications, and multimedia. The focus of this course will be on design methodologies for realization of dedicated VLSI systems for signal processing and communication applications. This will also include architectures for big-data computing and machine learning. The design methodologies will be used for exploring area-power-speed tradeoffs for different DSP applications. Apart from achieving capacity to process high speed data, minimization of area is another important constraint in VLSI implementations. Similarly, power consumption reduction is crucial in design of modern systems for portable as well as non-portable applications. This course will discuss power reduction techniques applicable to machine learning. Also, machine learning systems often do not require exact computing. To this end, approximate computing approaches will be discussed. Emerging stochastic logic based and stochastic computing based architectures will be presented. Also, emerging computing methods for hardware security will be discussed.

The course will be divided into two modules as given below :

Module A : High Level Transformations

Contents : Representation of digital signal processing systems: block diagrams, signal flow graphs, data-flow graphs, dependence graphs; pipelining and parallel processing for high-speed and low power realizations; iteration bound, algorithms to compute iteration bound, retiming of data-flow graphs; unfolding transformation of data-flow graphs; folding transformation of data-flow graphs and design of time-multiplexed architectures; numerical strength reduction, algorithm-level strength reduction, fast convolution, parallel FIR filters; systolic architecture design, architectures for real and complex fast Fourier transforms using folding; arithmetic implementations: addition and multiplication using carry-ripple and carry-save, canonic signed digit multiplication; redundant number representation, redundant multiplication, fast binary addition.

Module B : Architectures for internet infrastructures, hardware security and machine learning

Contents : Architectures for Viterbi decoders, fixed-width multiplication; architectures for low-energy support vector machines, restricted Boltzmann machine; pipelining of quantizer loops, pipelined and parallel architectures for decision feedback equalizers; parallel decision feedback decoders and applications to gigabit ethernet; pipelining of the Tomlinson-Harashima precoder and application to 10-gigabit ethernet standard; stochastic logic based computing, computing digital filters, arithmetic functions and machine learning functions using stochastic computing; hardware security, physical unclonable functions, robust authentication, obfuscation of integrated circuits, preventing reverse engineering and piracy of intellectual property.

Modules		
	A: High Level Transformations :	Dec.19 – 23, 2016
	B: Architectures for internet infrastructures, hardware security and machine learning	Dec. 26 – 30, 2016

Number of seats will be limited and prospective candidates should apply early.

Who Can Attend

- Faculty members from engineering colleges / universities with interests in VLSI design optimization of signal processing and communication algorithms.
- Research scholars, M.E./M.Tech. and senior B.E./B.Tech. students from electronics, electrical and communications engineering and computer science.
- Engineers from industry and scientists from research labs working in areas like DSP implementation, digital hardware design, VLSI design etc.

Fees

Registration fees for attending the course are as follows:

Participants from abroad : US $500 for either module; US $750.00 for the two modules together

Participants from industry within India: 20000.00 for either module; 30000.00 for the two modules together

Scientists from DRDO/ISRO : 15000.00 per module (30000.00 for the two modules together)

Faculty/staff from academic institutions within India : 10000.00 for either module; 15000.00 for the two modules together

Bonafide students from academic institutions within India : Rs. 1000.00 (to be refunded on completion of course)

The above fees include service tax, if any. Additionally, it covers all instructional materials, tutorials and assignments, laboratory equipment usage, 24 hr free internet facility. The participants may be provided with accommodation on payment basis.

The Faculty

Keshab K. Parhi received B.Tech. degree from the Indian Institute of Technology (IIT), Kharagpur in 1982, the M.S.E.E. degree from the University of Pennsylvania, Philadelphia in 1984, and the Ph.D. degree from the University of California, Berkeley in 1988. He has been with the University of Minnesota, Minneapolis, since 1988, where he is currently the Distinguished McKnight University Professor and Edgar F. Johnson Professor in the Department of Electrical and Computer Engineering. He has published over 550 papers, has authored the textbook VLSI Digital Signal Processing Systems (Wiley, 1999) and co-edited the reference book Digital Signal Processing for Multimedia Systems (Marcel Dekker, 1999). Dr. Parhi is widely recognized for his work on high-level transformations of iterative data-flow computations and for developing a formal theory of computing for design of digital signal processing systems. His current research addresses VLSI architecture design and implementation of signal processing, communications and biomedical systems, error control coder and cryptography architectures, high-speed transceivers, stochastic computing, secure computing, and molecular computing. He is also currently working on intelligent classification of biomedical signals and images, for applications such as seizure prediction and detection, schizophrenia classification, biomarkers for mental disorder, brain connectivity, and diabetic retinopathy screening. Dr. Parhi is the recipient of numerous awards including the 2013 Distinguished Alumnus Award from IIT, Kharagpur, the 2013 Graduate/Professional Teaching Award from the University of Minnesota, the 2012 Charles A. Desoer Technical Achievement award from the IEEE Circuits and Systems Society, the 2004 F. E. Terman award from the American Society of Engineering Education, the 2003 IEEE Kiyo Tomiyasu Technical Field Award, the 2001 IEEE W. R. G. Baker prize paper award, and a Golden Jubilee medal from the IEEE Circuits and Systems Society in 2000. He was elected a Fellow of IEEE in 1996. He served as the Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS —PART I (2004-2005 term), as technical program cochair of the 1995 IEEE VLSI Signal Processing workshop and the 1996 ASAP conference, and as the general chair of the 2002 IEEE Workshop on Signal Processing Systems. He was a distinguished lecturer for the IEEE Circuits and Systems society during 1996-1998. He served as an elected member of the Board of Governors of the IEEE Circuits and Systems society from 2005 to 2007.

Mrityunjoy Chakraborty obtained Bachelor of Engg. from Jadavpur university, Calcutta, Master of Technology from IIT, Kanpur and Ph.D. from IIT, Delhi. He joined IIT, Kharagpur as a faculty member in 1994, where he currently holds the position of a professor in Electronics and Electrical Communication Engg. The teaching and research interests of Prof. Chakraborty are in Digital and Adaptive Signal Processing, VLSI Signal Processing, Linear Algebra and Compressive Sensing. In these areas, Prof. Chakraborty has supervised several graduate theses, carried out independent research and has several well cited publications.

Prof. Chakraborty is currently a senior editorial board member of the IEEE Signal Processing Magazine and also of the IEEE journal of Emerging Techniques in Circuits and Systems. Earlier, he had been an Associate Editor of the IEEE Transactions on Circuits and Systems, part I (2004-2007, 2010-2012) and part II (2008-2009), apart from being an elected member (also currently the chair) of the DSP Technical Committee (TC) of the IEEE Circuits and Systems Society, a guest editor of the EURASIP JASP, track co-chair (DSP track) of ISCAS 2015-2017, Gabor track chair of DSP-15, and a TPC member of ISCAS (2011-2014), ICC (2007-2011) and Globecom (2008-2011). Prof. Chakraborty is a co-founder of the Asia Pacific Signal and Information Processing Association (APSIPA), is currently a member of the APSIPA BOG and also, served as the chair of the APSIPA TC on Signal and Information Processing Theory and Methods (SIPTM). He has also been the general chair and also the TPC chair of the National Conference on Communications – 2012.

Prof. Chakraborty is a fellow of the National Academy of Science, India, and also of the Indian National Academy of Engineering (INAE). During 2012-2013, he was selected as a distinguished lecturer of the APSIPA.

Course Co-ordinator

Prof. Mrityunjoy Chakraborty

Phone: 03222-283512,

Mobile : +91-9434026874

E-mail: mrityun@ece.iitkgp.ernet.in

http://www.gian.iitkgp.ac.in/GREGN

Registration Process

Registration and payment of fees is to be carried out online as per the following :

1. **Create login and password at www.cep.iitkgp.ac.in/gian**
2. **Login and fill out the registration form [if you already had registered earlier, you can skip steps 1 & 2 and go directly to step 3].**
3. **Select the course**
4. **Confirm your application and payment information.**
5. **Pay Rs. 500.00 through online payment gateway. This is a one-time lifetime registration fee. With this, you can apply for as many courses as possible on the GIAN website.**

The course coordinator will go through your application and confirm your selection as a participant one month before the starting date of the course. Once you are selected, you will be informed and requested to pay the full fees through online payment gateway service.

htt://www.cep.iitkgp.ac.in/gian