INVITATION FOR TENDER FOR SUPPLY OF EQUIPMENT

Sealed tender offers are invited in two separate sealed covers (Technical and Commercial offers) from eligible manufacturers/suppliers or their direct Indian agents for the supply of the following equipment.

Sl. No	Items	Quantity	Unit Price	Total Price
1	**Xilinx Virtex- 7 FPGA VC707 Evalution Kit**	**4**		
2	**Nexys 4 FPGA Board**	**10**		
3	**JTAG Programmer**	**5**		
4	**Xillinx Vivado 25 user along with DPR licence for 5 users**	**1**		

Please send offers, ALONG WITH DESCRIPTIVE CATALOGUE/ BROCHURE. The validity of the bid should be at least four months (120 days) or more from the date of the opening of this tender. Please ensure that your quotation reaches not later than **18.05.2018 at 15:00 Hrs** at the following address:

Dr. Debdeep Mukhopadhyay, Professor, Computer Science and Engineering Department
Indian Institute of Technology Kharagpur – 721 302, West Bengal, India

Earnest money of **Rs. 30,000/-** is to be deposited in the form of Account payee Demand Draft in favour of IIT Kharagpur, payable at Kharagpur, India. Any bid which is not accompanied with an EMD shall be summarily rejected. Earnest money deposited will be forfeited if the tenderer withdraws or amends its tender or impairs or derogates from the tender in any respect within the period of validity of its tender. No interest will be paid on the earnest money of the unsuccessful bidders.

Tender Reference	**IIT/SRIC/CSE/NUS/DM/2017-18/EQ-4, Dated:23.04.2018**
Price of Tender Document	**NIL**
Last Date and Time for submitting the tender document	**18.05.2018 at 15:00 Hrs (Indian time)**
Time and Date of Opening of Technical Bids	**18.05.2018 at 16:30 Hrs (Indian time)**
Place of Opening Tender	**Computer Science and Engineering Department, Indian Institute of Technology Kharagpur – 721 302, West Bengal, India**
Address of Communication	**As stated above**
Contact Telephone Numbers	**+91- 3222 - 282352**
E-mail	**debdeep@cse.iitkgp.ernet.in**

DETAILED TECHNICAL SPECIFICATIONS FOR

1. Xilinx Virtex- 7 FPGA VC707 Evalution Kit

Virtex-7 XC7VX485T-2FFG1761C FPGA

1. 1 GB DDR3 memory SODIMM
2. 128 MB Linear byte peripheral interface (BPI) Flash memory
3. USB 2.0 ULPI Transceiver
4. Secure Digital (SD) connector
5. USB JTAG through Digilent module
6. Clock Generation
   - Fixed 200 MHz LVDS oscillator (differential)
   - I2C programmable LVDS oscillator (differential)
   - SMA connectors (differential)
   - SMA connectors for GTX transceiver clocking
7. GTX transceivers
   - FMC1 HPC connector (eight GTX transceivers)
   - FMC2 HPC connector (eight GTX transceiver)
   - SMA connectors (one pair each for TX, RX, and REFCLK)
   - PCI Express (eight lanes)
   - Small form-factor pluggable plus (SFP+) connector
   - Ethernet PHY SGMII interface (RJ-45 connector)
8. PCI Express endpoint conne
   - Gen1 8-lane (x8)
   - Gen2 8-lane (x8)
9. SFP+ Connector
10. 10/100/1000 tri-speed Ethernet PHY
11. USB-to-UART bridge
12. HDMI™ codec
13. I^2C bus
    - I^2C MUX
    - I^2C EEPROM (1 KB)
    - USER I^2C programmable LVDS oscillator
    - DDR3 SODIMM socket
    - HDMI codec
    - FMC1 HPC connector
    - FMC2 HPC connector

- SFP+ connector
- I²C programmable jitter-attenuating precision clock multiplier

14. Status LEDs
    - Ethernet status
    - Power good
    - FPGA INIT
    - FPGA DONE
15. User I/O
    - User LEDs (eight GPIO)
    - User pushbuttons (five directional)
    - CPU reset pushbutton
    - User DIP switch (8-pole GPIO)
    - User SMA GPIO connectors (one pair)
    - LCD character display (16 characters x 2 lines)
16. Switches
    - Power on/off slide switch
    - FPGA_PROB_B pushbutton
    - Configuration mode DIP switch
17. VITA 57.1 FMC1 HPC Connector
18. VITA 57.1 FMC2 HPC Connector
19. Power management
    - PMBus voltage and current monitoring through TI power controller
20. XADC header
21. Configuration options
22. Linear BPI Flash memory
23. USB JTAG configuration port
24. Platform cable header JTAG configuration port

2. Nexys 4 FPGA Board

The Nexys4 DDR board is a complete, ready-to-use digital circuit development platform based on the latest Artix-7™ Field Programmable Gate Array (FPGA) from Xilinx®. With its large, high-capacity FPGA (Xilinx part number XC7A100T-CSG324C), generous external memories, and collection of USB, Ethernet, and other ports, the Nexys4 DDR can host designs ranging from introductory combinational

circuits to powerful embedded processors. Several built-in peripherals, including an accelerometer, temperature sensor, MEMs digital microphone, a speaker amplifier, and several I/O devices allow the Nexys4 DDR to be used for a wide range of designs without needing any other components. The Artix-7 FPGA is optimized for high performance logic, and offers more capacity, higher performance, and more resources than earlier designs. Artix-7 100T features include:

- 15,850 logic slices, each with four 6-input LUTs and 8 flip-flops
- 4,860 Kbits of fast block RAM
- Six clock management tiles, each with phase-locked loop (PLL)
- 240 DSP slices
- Internal clock speeds exceeding 450 MHz
- On-chip analog-to-digital converter (XADC)

The Nexys4 DDR also offers an improved collection of ports and peripherals, including:

• 16 user switches	• 16 user LEDs	• Two 4-digit 7-segment displays
• USB-UART Bridge	• Two tri-color LEDs	• Micro SD card connector
• 12-bit VGA output	• PWM audio output	• PDM microphone
• 3-axis accelerometer	• Temperature sensor	• 10/100 Ethernet PHY
• 128MiB DDR2	• Serial Flash	• Four Pmod ports
• Pmod for XADC signals	• Digilent USB-JTAG port for FPGA programming and communication	• USB HID Host for mice, keyboards and memory sticks

The Nexys4 DDR is compatible with Xilinx's new high-performance Vivado® Design Suite as well as the ISE® toolset,which includes ChipScope™ and EDK. Xilinx offers free WebPACK™ versions of these toolsets, so designs can be implemented at no additional cost. The Nexys4 DDR is not supported by the Digilent Adept Utility .

3. JTAG Programmer

The Platform Cable USB II provides integrated firmware to deliver high-performance, reliable and user-friendly configuration of Xilinx FPGAs and programming of Xilinx PROM and CPLD devices. The Platform Cable USB II cable optimizes direct programming of third-party SPI flash memory devices and indirect programming of SPI or parallel NOR flash memory devices via the FPGA JTAG port. In addition, Platform Cable USB II is a cost effective tool for debugging embedded software and firmware when used with Xilinx applications such as the Embedded Development Kit and ChipScope™ Pro Analyzer.

Platform Cable USB II is an upgrade to and backwards compatible with Platform Cable USB. It has industry-leading performance and is compatible with Full Speed (USB 1.1) and Hi-Speed (USB 2.0) ports.

4. Xillinx Vivado 25 user along with DPR licence for 5 users

The following UltraScale+™ devices are in production:

- Kintex® UltraScale+:
    - ° XCKU3P, XCKU5P, XCKU9P
- Virtex® UltraScale+:
    - ° XCVU3P
- Zynq® UltraScale+ MPSoC:
    - ° XCZU2EG/CG, XCZU3EG/CG, XCZU6EG/CG, XCZU9EZG/CG
- Spartan®-7 devices are introduced in this release:
    - ° XC7S50

This release enables initial Vivado WebPack support for UltraScale+:

- Kintex UltraScale+:
    - ° XCKU3P, XCKU5P
- Zynq UltraScale+ MPSoC:
    - ° XCZU2EG/CG, XCZU3EG/CG

Enhancements to the math.h library.

    - Added functions for complete coverage.
    - New native optimized support for half-precision floating point.

- Dataflow pragma supports loops with variable bounds.
- User assistance functionality enabled in co-simulation for ease of use.

System Generator for DSP

- Supported MATLAB Versions: R2016a, R2016b, and R2017a.
- New MRI Image Reconstruction with 2D-FFT demo.
- Enhancements to Digital Filtering and Digital Communications demos.

GENERAL TERMS & CONDITIONS

PLEASE SPECIFICALLY INDICATE THE FOLLOWING POINTS IN YOUR QUOTATIONS AND COMPLY THE TERMS AS MENTIONED HEREUNDER:-

1. TENDER ARE INVITED COMPLYING THE REQUIREMENT FOR TENDER AS DETAILED IN THE TENDER SPECIFICATION TO BE SUBMITTED IN THE COMPANY'S / FIRM'S LETTERHEAD NEATLY PRINTED / TYPED DULY SIGNED BY AUTHORIZED PERSON WITH THE SEAL OF THE BIDDERS. ALL ENVELOPS CONTAINING THE TENDER SHOULD BE PROPERLY SEALED. SEPARATE ENVELOPS SHOULD BE USED FOR TECHNICAL AND PRICE BID AND INDICATION TO THEIR EFFECT MAY PLEASE BE SUPERSCRIBED ON THE ENVELOP.

THE FOLLOWING DOCUMENTS ARE REQUIRED FROM THE INDIAN AGENTS OF FOREIGN FIRMS:

1.1 FOREIGN PRINCIPAL'S PROFORMA INVOICE INDICATING THE COMMISSION PAYABLE TO THE INDIAN AGENT AND NATURE OF AFTER SALES SERVICE TO BE RENDERED BY THE INDIAN AGENT.

1.2 COPY OF THE AGENCY AGREEMENT WITH THE FOREIGN PRINCIPAL INDICATING THE NATURE OF AFTER SALES SERVICES, PRECISE RELATIONSHIP BETWEEN THEM AND THEIR MUTUAL INTEREST IN THE BUSINESS.

1.3 PLEASE ENCLOSE THE DOCUMENT(S) RELATED TO THE ENLISTMENT OF THE INDIAN AGENT WITH DIRECTOR GENERAL OF SUPPLIES & DISPOSALS (DGS & R) UNDER THE COMPULSORY REGISTRATION SCHEME OF MINISTRY OF FINANCE.

2. TECHNICAL CATALOGUE/LEAFLET SHOULD BE ENCLOSED WITHOUT FAIL. PROVIDE COMPLIANCE STATEMENT WITH RESPECT TO THE TECHNICAL SPECIFICATIONS MENTIONED ABOVE.

3. PLEASE CONFIRM WHETHER YOU ARE AUTHORISED TO QUOTE ON BEHALF OF YOUR PRINCIPALS AND IF SO, PLEASE ENCLOSE A COPY OF SUCH AUTHORISATION WITH YOUR QUOTATION.

4. **PRICE BIDS FOR FOREIGN FIRMS**: PRICES ARE TO BE QUOTED ON '**EX-WORKS**' DULY PACKED OR ON **"FCA/FOB"** INTERNATIONAL PORT" BASIS AND ALSO INCLUDING AGENCY COMMISSION PAYABLE TO YOUR INDIAN AGENTS, IF ANY SHOWING CLEARLY THE FOLLOWING BREAK UP:-

   I) EX-WORKS PRICE
   II) PACKING & FORWARDING
   III) FREIGHT
   IV) ANY OTHER RELEVANT EXPENSES.
   V) TAXES PAYABLE BY THE INSTITUTE

   INSURANCE WILL BE PAID BY OUR INSTITUTE SEPARATELY AND SHOULD NOT FORM PART OF THE QUOTED PRICE.

   PRICE BIDS FOR INDIAN FIRMS: PRICES ARE TO BE QUOTED ON F.O.R., IIT KHARAGPUR, ON DOOR DELIVERY BASIS CLEARLY SHOWING THE BREAK UP.

5. **PERIOD OF VALIDITY**: BIDS SHALL REMAIN VALID FOR ACCEPTANCE FOR A PERIOD OF 120 DAYS FROM THE DATE OF OPENING.

6. INDIAN AGENTS ADDRESS AND PERCENTAGE OF AGENCY COMMISSION INCLUDED IN ABOVE F.O.B./EX-WORKS PRICE. (THIS WILL BE PAID TO THE INDIAN AGENTS IN INDIAN RUPEES ONLY AND NOT IN **FE).** PLEASE ENCLOSE COPY OF AGENCY AGREEMENT ENTERED INTO WITH YOUR PRINCIPALS INDICATING THE NATURE OF AFTER SALES SERVICES OF INDIAN AGENTS, PRECISE RELATIONSHIP & MUTUAL INTEREST IN THE BUSINESS.

7. **MEASUREMENTS/WEIGHT:** NETT/GROSS OF THE CONSIGNMENT. IN CASE OF AN ORDER, YOU SHALL USE AIR WORTHY PACKAGE (AS APPLICABLE) DULY CERTIFIED WITH DOCUMENTS – PLYTO – SANITARY CERTIFICATE (AS PER QUARANTINE ORDER 2003).

8. **SCOPE OF SUPPLY**: SHOULD INCLUDE FREE INSTALLATION AND COMMISSIONING

9. **PAYMENT TERMS** FOR FOREIGN FIRMS

   The offer will be made on a single currency and only one PO will be issued for the entire scope of the supply.

   A) 90% PAYMENT THROUGH SIGHTDRAFT/FORIGN DEMAND DRAFT/LC (EXCEPTIONAL CASES)/SWIFT TELE TRANSFER AFTER RECEIPT OF STORE IN GOOD ORDER AND CONDITION AND 10% AFTER SUCCESSFUL INSTALLATION & COMMISSIONING.

   B) BANK CHARGES ON LC/SD (WITHIN INDIA APPLICANT ACCOUNT AND OUTSIDE INDIA TO BENEFICIARY ACCOUNT).

   PAYMENT TERMS FOR INDIAN FIRMS

   A) 100% PAYMENT THROUGH CROSSED ACCOUNT PAYEE CHEQUE / ELECTRONIC TRANSFER AFTER RECEIPT OF STORE IN GOOD ORDER & CONDITION AND SUCCESSFUL INSTALLATION & COMMISSIONING.

   B) ENSURE MENTIONING

   i) BANK DETAILS OF THE BENEFICIARY, GST NO. AND PAN NUMBER

   ii) FULL NAME AND ADDRESS OF THE BENEFICIARY ON WHOM ORDER HAS TO BE PLACED

10. WHETHER ANY EXPORT LICENCE IS REQUIRED FROM YOUR GOVERNMENT, IF SO, PLEASE CONFIRM WITH DETAILS.

11. COUNTRY OF ORIGIN OF THE GOODS IS TO BE MENTIONED.

12. THE INSTITUTE SHALL PROVIDE THE CONCESSIONAL CUSTOMS DUTY AND EXCISE DUTY EXEMPTION CERTIFICATE AS PER GOVT. NOTIFICATION NO. 51/96 CUSTOMS DATED: 23.07.1996 AND CENTRAL EXCISE DUTY EXCEMPTION IN TERMS OF GOVT. NOTOFICATION NO. 10/97 – CENTRAL EXCISE DATED: 01.03.1997 AS AMENDED FROM TIME TO TIME.

13. **LIQUIDATED DAMAGES**: THE STORES SHOULD BE DELIVERED / DISPATCHED TO DESTINATION AND READY FOR OPERATION NOT LATER THAN THE DELIVERY DATE SPECIFIED. IT THE SUPPLIER FAILS TO DELIVER ANY OR ALL THE STORES OR PERFORM THE SERVICE BY THE SPECIFIED DATE, LIQUIDATED DAMAGES AT 1% PER MONTH OR PART THEREOF IN RESPECT OF THE VALUE OF STORES WILL BE DEDUCTED FROM THE CONTRACT PRICE SUBJECT TO A MAXIMUM OF 5%. ALTERNATIVELY, THE ORDER WILL BE CANCELLED AND THE UNDELIVERED STORES PURCHASED FROM ELSEWHERE AT THE RISK AND EXPENSE OF SUPPLIER.

14. **PATENT RIGHTS**: THE SUPPLIER SHALL INDEMNIFY THE PURCHASE AGAINST ALL THIRD PARTY CLAIMS OF INFRINGEMENT OF PATENT, TRADEMARK OR INDUSTRIAL DESIGN RIGHTS ARISING FROM USE OF THE GOODS OR ANY PART THEREOF IN INDIA.

15. ONLY THOSE BIDDERS WHO'S BIDS HAVE BEEN TECHNICALLY FOUND ACCEPTABLE WILL ONLY BE INVITED FOR PARTICIPATION IN THE PRICE BID.

16. THOSE BIDDERS WHO DO NOT RECEIVE ANY COMMUNICATION FOR PARTICIPATION IN PRICE BID OPENING MEETING MAY PRESUME THAT THEIR BID HAS NOT BEEN ACCEPTED BY THE INSTITUTE.
17. CONDITIONAL OFFER WILL NOT BE ACCEPTED.

18. LATE TENDERS I.E. TENDER RECEIVED AFTER THE DUE DATE AND TIME OF SUBMISSION AS MENTIONED ABOVE SHALL NOT BE ACCEPTED.

19. BIDDERS TO ENCLOSE THE FOLLOWING DOCUMENTS:-

    A) CURRENT INCOME TAX AND SALES TAX CLEARANCE CERTIFICATES (GST No.), AND PAN NO.

    B) BANKER'S SOLVENCY CERTIFICATE

    C) SUMMARY OF AUDITED STATEMENT OF ACCOUNTS FOR THE LAST THREE YEARS TO BE ENCLOSED AND FINANCIAL HIGHLIGHTS AND THE KEY PERFORMANCE DURING THE LAST THREE QUARTERS TO BE ENCLOSED AS PER FORMAT:-

COMPANY'S KEY PERFORMANCE

DESCRIPTION	JAN. TO MARCH	APRIL TO JUNE	JULY TO SEPT.
GROSS REVENUE			
PROFIT BEFORE TAX			
PROFIT AFTER TAX			
RETURN ON INVESTED			
CAPITAL (ROIC)			

D) CUSTOMER SATISFACTION CERTIFICATE FROM ONE SUCH ORGANIZATION IS TO BE ATTACHED WITH THE TECHNICAL BID AND PRICE BID.

E) NAME AND ADDRESS OF MINIMUM THREE CLIENTS TO WHOM SUCH EQUIPMENT HAVE BEEN SUPPLIED SHOULD BE MENTIONED.

20. **WARRANTY / GUARANTEE**: COMPREHENSIVE WARRANTY OF THE COMPLETE SYSTEM SHOULD BE **36 MONTHS FROM THE DATE OF SUCCESSFUL INSTALLATION & HANDOVER, AND 24 MONTHS OPTIONAL EXTENDED WARRANTY** AFTER THE GOODS (OR ANY PORTION THEREOF AS THE CASE MAY BE) HAVE BEEN DELIVERED AND COMMISSIONED TO THE FINAL DESTINATION.

21. THE INSTITUTE DOES NOT BIND ITSELF TO OFFER ANY EXPLANATION TO THOSE BIDDERS WHO'S TECHNICAL BID HAS NOT BEEN FOUND ACCEPTABLE BY THE EVALUATION COMMITTEE OF THE INSTITUTE.

22. ALL TENDERS (UNLESS OTHERWISE SPECIFIED) ARE TO BE SUBMITTED / HANDED OVER TO **DR. DEBDEEP MUKHOPADHYAY, PROFESSOR, COMPUTER SCIENCE AND ENGINEERING DEPARTMENT, INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR - 721 302** AND ACKNOWLEDGEMENT TO BE OBTAINED.

IMPORTANT

1. IIT Kharagpur authority may accept or reject any or all the bids in part or in full without assigning any reason and does not bind itself to accept the lowest bid. The Institute at its discretion may change the quantity / upgrade the criteria / drop any item or part thereof at any time before placing the Purchase Order.

2. Promptly make arrangements for repair and / or replacement of any damaged item (s) irrespective of settlement of claim.

3. In case of any dispute, the decision of the Institute authority shall be final and binding on the bidders.

4. For any query pertaining to this bid document correspondence may be addressed to **Dr. Debdeep Mukhopadhyay, Professor, Computer Science and Engineering Department** at the address mentioned above.

LAST DATE FOR SUBMISSION OF SEALED BIDS: 18.05.2018

1) Please Note that the Institute remains closed during Saturdays & Sundays and all specified government holidays.

2) Fax, e-mail Tender will not be accepted.

3) The General Terms and Conditions as stated above relate to supply of stores / equipment /assets etc. and for specific service other terms and conditions of the Institute will apply.
