INVITATION FOR TENDER FOR SUPPLY OF EQUIPMENT

Sealed tender offers are invited in two separate sealed covers (Technical and Commercial offers) from eligible manufacturers/suppliers or their direct Indian agents for the supply of the following equipment.

1. **2kW 70V DC to 230V AC Converter Quantity2**
2. **3kW 230V AC to 400V DC PFC Converter Quantity:2**
3. **3kW 70V DC to 230V AC Converter Quantity2**
4. **3kW 70V DC to 400V DC CSVS DAB Converter Quantity:2**

Please send offers, ONE TECHNICAL OFFER GIVING THE DESIGN CALCULATIONS FOR SELECTION OF POWER CIRCUIT COMPONENTS AND THE OTHER COMMERCIAL OFFER FOR PRICE for verification at IIT Kharagpur. The validity of the bid should be at least four months (120 days) or more from the date of the opening of this tender. Please ensure that your quotation reaches not later than **31.01.2019 at 15:00 Hrs** at the following address:

Dr. Souvik Chattopadhyay,
Assistant Professor , Department of Electrical Engineering,
Indian Institute of Technology Kharagpur – 721 302, West Bengal, India

Earnest money of **NIL** is to be deposited in the form of Account payee Demand Draft in favour of IIT Kharagpur, payable at Kharagpur, India. Any bid which is not accompanied with an EMD shall be summarily rejected. Earnest money deposited will be forfeited if the tenderer withdraws or amends its tender or impairs or derogates from the tender in any respect within the period of validity of its tender. No interest will be paid on the earnest money of the unsuccessful bidders.

Tender Reference	**IIT/SRIC/EE/ESU/SC/18-19/CON-16 , Dated: 19.12.2018**
Price of Tender Document	**NIL**
Last Date and Time for submitting the tender document	**31.01.2019 at 15:00 Hrs (Indian time)**
Time and Date of Opening of Technical Bids	**07.02.2019 at 16:00 Hrs (Indian time)**
Place of Opening Tender	**Department of Electrical Engineering, Indian Institute of Technology Kharagpur – 721 302, West Bengal, India**
Address of Communication	**As stated above**
Contact Telephone Numbers	**+91- 3222 - 283048**
E-mail	**souvik@ee.iitkgp.ernet.in**

GUIDELINES TO BE FOLLOWED (READ THIS FIRST)

The objective of this tender is to receive quotation for well designed and robustly engineered power converter hardware blocks that would be required for the development of lab prototypes. The application area is EV charger with solar and battery/super capacitor interface. It may be noted that in each case the item to be delivered is not intended to be a fully functional unit. Instead, it is expected to be a power block with associated switching devices, gate drives, magnetic circuit components, thermal assembly (with heatsink/fan) and voltage and current sensors along with the protection circuits. The control voltage power supply (+12V,-12V,5V) is to be included in the deliverables. The power terminal blocks for input and output supply connections would have to be provided. A relay-contactor unit for isolation of the external power supply/load would be necessary. It is expected that this power block (at least most of the components) essentially resides in a printed circuit board. However, magnetic circuit components may be placed (and clamped) on a separate fixture such as an aluminium plate to save board space and ease of circuit layout.

Based on the simulation of each of these converters this document has provided quite a few specific component values and also suggested the part numbers of components that may be selected for the design of the converter. Though it is not mandatory but the vendors are advised to choose the part numbers mentioned in this document. In case of any deviation a justification has to be provided in the technical bid (separate from price bid). During the quotation phase, the simulation file may also be provided to the vendor for technical support, provided they send a request for it. Also, it case of any doubt, the prospective supplier is encouraged to establish an email contact with Dr. Souvik Chattopadhyay for seeking any clarification on the specification of the converters given below. It is to be noted that the quote must contain a technical document in a separate folder (from the price bid) indicating the actual selection of the components in terms of part numbers and/or other related information. The vendor who would supply these power converters has to provide a test certificate confirming the steady state open-loop operation at rated voltage and rated current.

1. 2kW 70V DC to 230V AC Converter

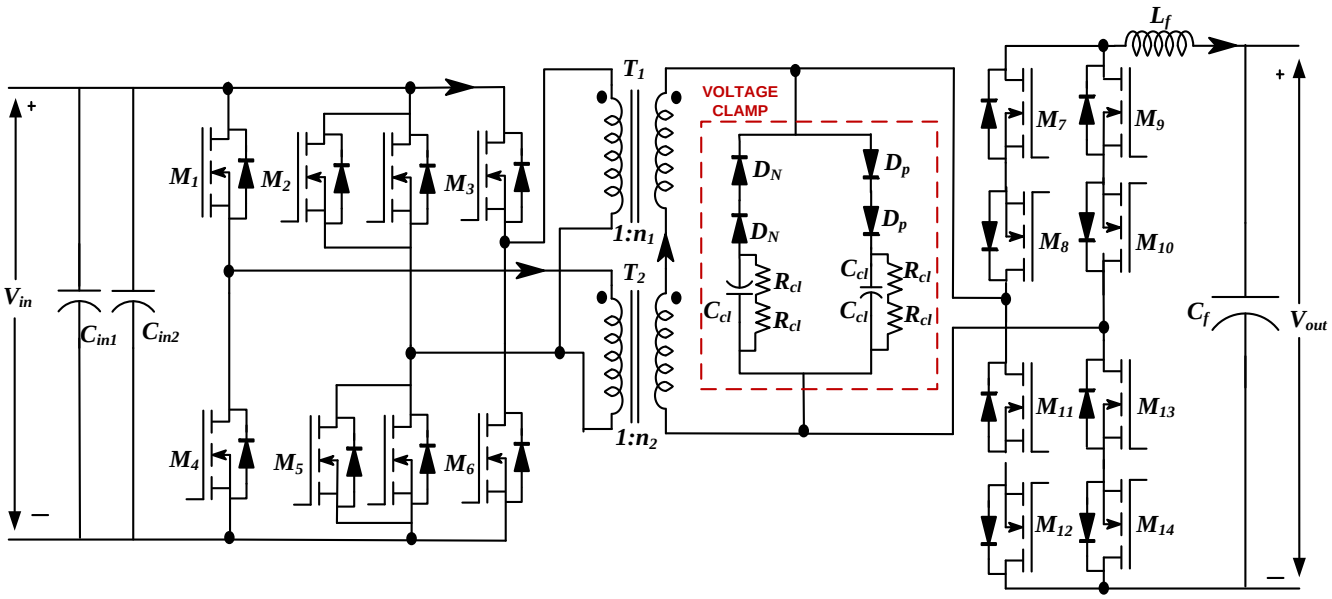


Figure 1 Circuit diagram of the DC to DC Converter

Converter Specification	
Parameter	***Value***
Rated output power	2kW
Nominal input voltage	70V DC
Nominal output voltage	230V, 50Hz, 1 phase AC
Switching frequency	50kHz
Input Capacitance, C_{in1}	100uF, 100V (10 Capacitors each of MKT 1820 *Vishay*)
Input Capacitance, C_{in2}	4mF, 100V (4 electrolytic Capacitors 1000uF 100V)

Mosfets, M_1,M_2,M_3,M_4,M_5,M_6	*Infineon* IRFP4668PBF Note: M_2 and M_5 are to be realized by connecting two MOSFETs in parallel as shown in the figure
Mosfets, M_7,M_8,M_9,M_{10},M_{11},M_{12}	*Cree* C2M0040120D, SiC based
Secondary filter inductance, L_f	3mH,8.6A (RMS), Maximum DC resistance = 0.1Ohm, $R_{ac}(50Hz)/R_{dc} < 1.05$
output side filter capacitors, C_f	2 uF, 1200V (2 capacitors of 1844 MKP *Vishay*)
Clamp Capacitor , C_{cl}	1uF, 1200V (1844 MKP *Vishay*)
Clamp Resistor, R_{cl}	100kOhm, 7W, 750V
Clamp Diode, D_N, D_P	*ST Rectifier*, STTH512D

High frequency transformer, T_1	Turns ratio (1: n_1) = 1:3.3, RMS Current through Primary = 23A, RMS Current through Secondary = 7A, Maximum Flux Density = 0.12T for Epcos N87Core material, 0.135T for FerroxCube 3C95 Material Leakage Inductance= As minimum as possible (less than 2uH), Magnetizing inductance (primary) (in uH) = 100uH Power Loss < 8W so that an efficiency of 99.2% can be obtained which implies that the total AC resistance at 50kHz referred to primary < 15mOhm. Suggestion: Generally the winding is done using copper foils or stranded copper litz wire. Anyone of them or some better technique can be used with the aim to achieve least possible leakage inductance and the desired efficiency.
High frequency transformer, T_2	Turns ratio (1: n_1) = 1:4.3, RMS Current through Primary = 30A, RMS Current through Secondary = 7A, Maximum Flux Density = 0.12T for Epcos N87Core material, 0.135T for FerroxCube 3C95 Material 0.11T for Cosmoferrite CF139 material Leakage Inductance= As minimum as possible (less than 2uH), Magnetizing inductance (primary) (in uH):As high as possible Power Loss < 12W so that an efficiency of 99.2% is obtained which implies that the total AC resistanceat 50kHz referred to primary < 13mOhm. Suggestion: Generally the winding is done using copper foils or stranded copper litz wire. Anyone of them or some better technique can be used with the aim to achieve least possible leakage inductance and the desired efficiency.,

Sensors	
1. Input voltage sensor	LEM LV 25 P or equivalent
2. Input current sensor	LEM LA 55 P or equivalent
3. Output voltage sensor	LEM LV 25 P or equivalent
4. Output current sensor	LEM LA 25 P or equivalent

CONTROLLER:

The control board and the control logic will be designed at IIT Kharagpur and therefore that is not in the scope of deliverables. However, the space and compatible connectors for placing and mounting the control board will have to be provided in the main printed circuit board. The dimension of the control board is provided in Figure 2. The power connector shown in the figure is a +5V connector.

This control connector with interface for the switching signals for device gate drives and isolated analog feedback signals from the sensors. The pin configuration is shown in Figure 3. The signals shown in red colors are input to the board and signals shown in blue color are outputs taken from the board.

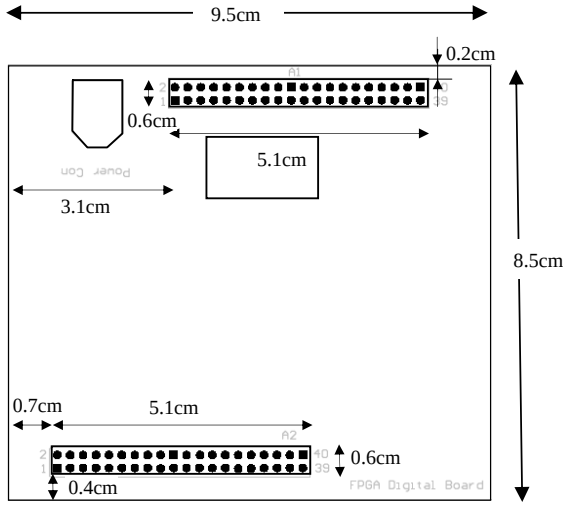


Figure 2 FPGA Board Dimensions

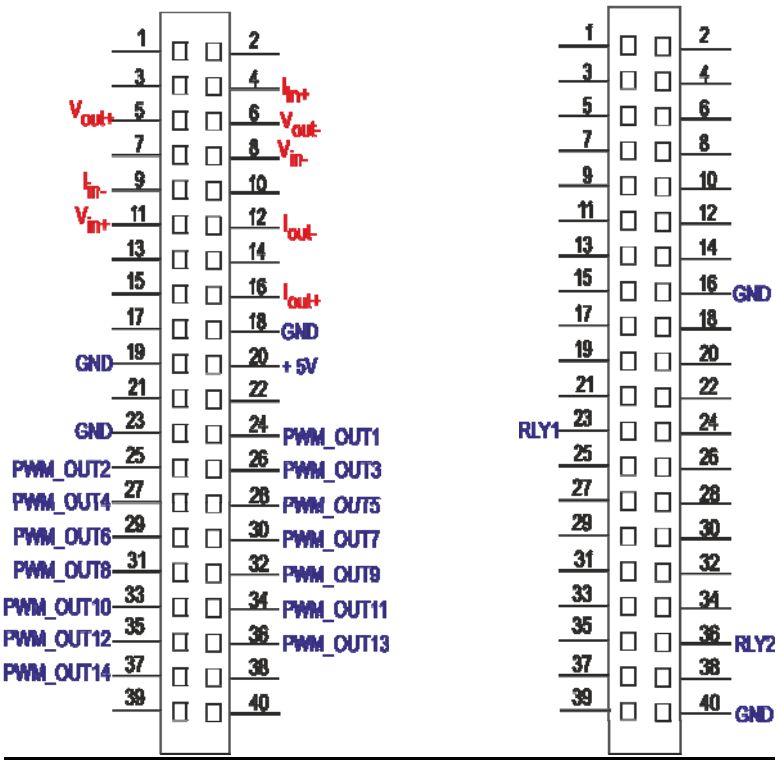


Figure 3 Dual Row 40 pin Female Header Connector for FPGA

Heatsinks
Primary side devices should be attached to the heat sink (OMNI-UNI-41-75, Wakefield Solutions) and be aircooled with fan (9GA0612PIK60, Sanyo Denki). Two devices should share one of these heat sinks. Similarly on the secondary side, two devices should share one heat sink (OMNI-UNI-41-75, Wakefield Solutions). The secondary side device need not be fan cooled. The heatsink temperature should not exceed 25 degree Celsius more than the ambient temperature.

Protection to be Incorporated
1. Over-voltage protection 2. Over current protection

2. 3kW 230V AC to 400V DC PFC Converter

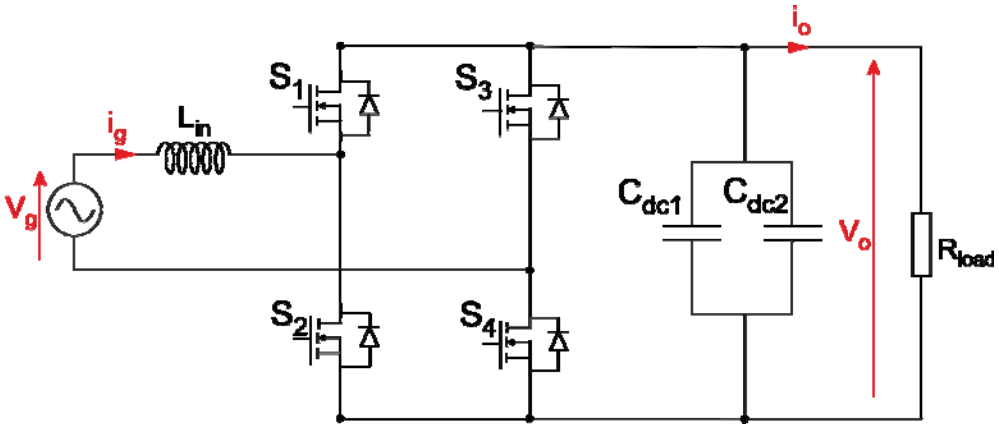


Figure 2: Circuit diagram of the PFC Converter

Converter Specification	
Parameter	***Value***
Rated output power	3 kW
Nominal input voltage	230V AC
Switching frequency	50kHz
Input inductance, Lin	1.5mH, 15A (RMS), Maximum resistance at 50Hz = 0.022Ohm,
Output capacitor, Cdc1,Cdc2	*200uF, 1100V (B32778J0207K000) each*
Mosfets, S1,S2,S3,S4	*Cree* C2M0040120D (1200V, 40 mohm), SiC based

Sensors:	
1. Input voltage sensor	LEM LV 25-P or equivalent
2. Input current sensor	LEM LA 25-P or equivalent
3. Output voltage sensor	LEM LV 25-P or equivalent
4. Output current sensor	LEM LA 25-P or equivalent
Heatsinks:	
Power semiconductor switches should be attached to the heat sink (OMNI-UNI-41-75, Wakefield Solutions). Two devices should share one of these heat sinks. The heatsink temperature should not exceed 25 degree Celsius more than the ambient temperature.	

Protections to be incorporated:
1. Over-voltage protection 2. Over current protection

Control signal requirments FPGA
The control board and the control logic will be designed at IIT Kharagpur and therefore that is not in the scope of deliverables. However, the space and compatible connectors for placing and mounting the control board (the dimensions and pin details are given in the figure below) will have to be provided in the main printed circuit board. This control connector will interface the switching signals for device gate drives and isolated analog feedback signals

from the sensors.

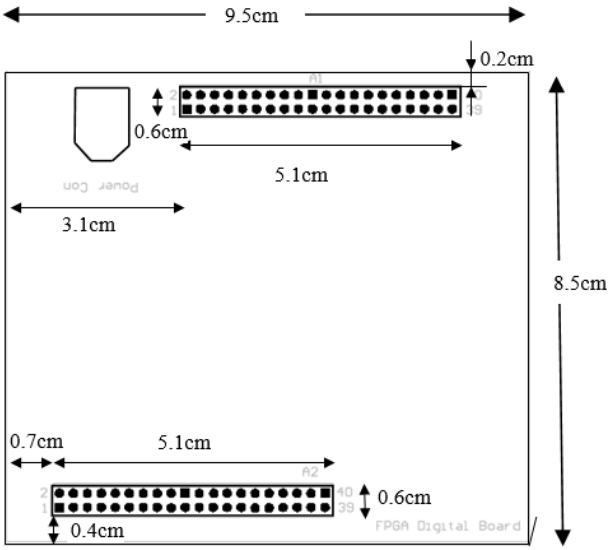
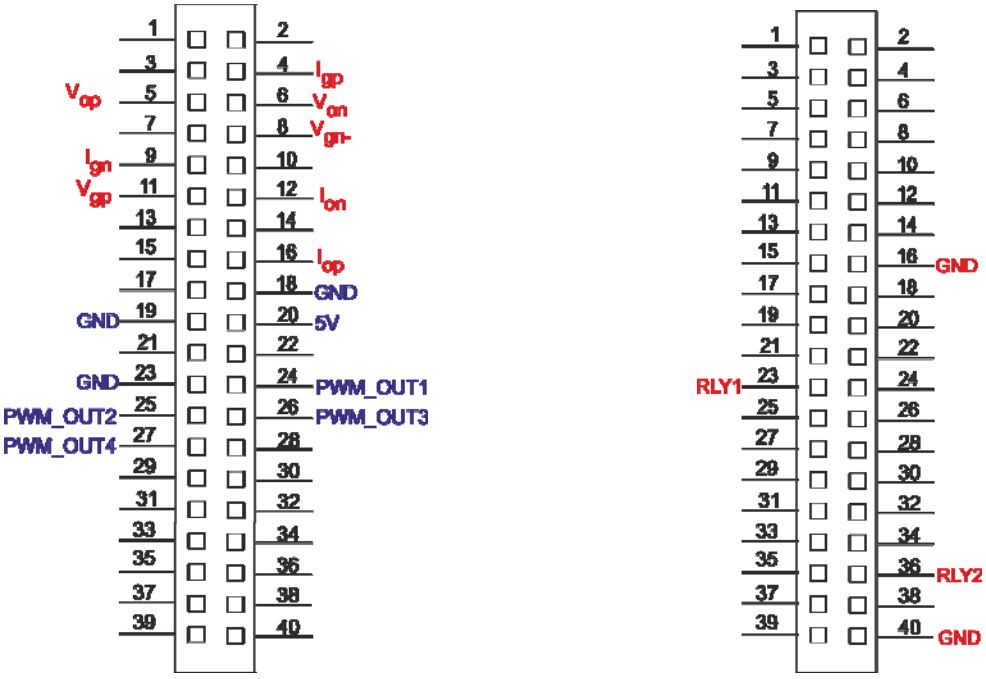


Figure 3 FPGA Board Dimensions



Connector 1 Connector 2

Fig.4. Dual row 40 pin female connector for FPGA

3. 3kW 70V DC to 230V AC Converter

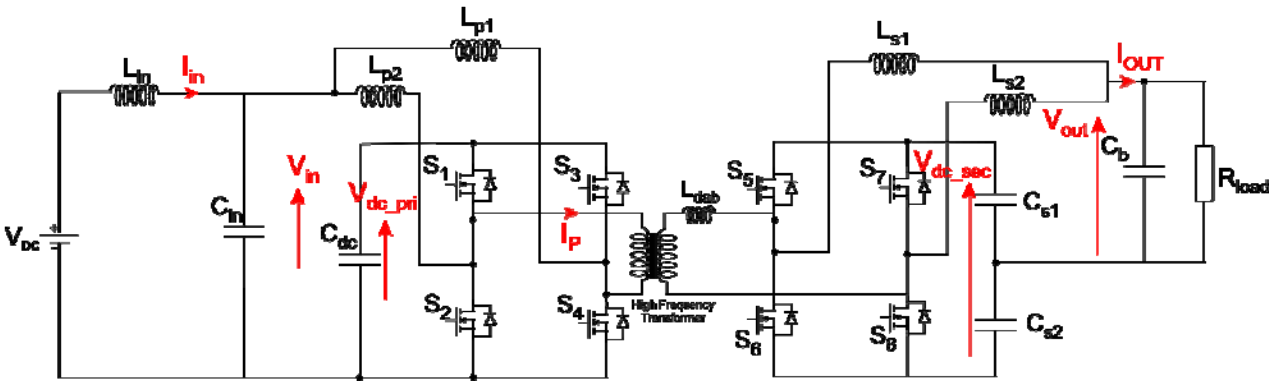


Figure 3: Circuit diagram of the DC to AC Converter

Converter Specification	
Parameter	***Value***
Rated output power	3kW
Nominal input voltage	70V DC
Nominal output voltage	230V, 50Hz AC
Switching frequency	50kHz
Mosfets, S1,S2,S3,S4	*Infineon* IRFP4668PBF
Input inductor, Lin	4uH, 44A(Avg), 52A(RMS), 72A peak to peak 100Hz ripple, $R_{ac}(100Hz)/R_{dc} < 1.05$
Input capacitor, Cin	*44uF, 450V (Two 22uF capacitors can be paralleled) (B32774D4226K000)*
DC side capacitor, Cdc	20uF,160V (B32676G1106 capacitors 2 in parallel)
High frequency transformer	Turns ratio (pri: sec) = 3:1, Core flux density must not exceed 0.1T
Mosfets, S5,S6,S7,S8	*Cree* C2M0040120D, SiC based
Dual active bridge inductor, Ldab	132.5uH (including transformer leakage inductance) , 0A (Avg), 15A(RMS), I_{peak} = 27A 54A peak to peak 50kHz ripple, $R_{ac}(50kHz):R_{dc} < 1.2$
Secondary inductance, Ls1,Ls2	1mH, 6.5A(RMS),I_{peak} =11A 3A peak to peak 50kHz ripple, $R_{ac}(50kHz)/Rdc <1.2$
AC side capacitors, Cs1,Cs2	200uF, 1100V (B32778J0207K000) each
Output capacitor, Cb	3.3uF, 230Vrms (C4AF3BW4330A3FK)

Sensors:	
1. Input voltage sensor	LEM LV 25-P or equivalent
2. Input current sensor	LEM LA 55-P or equivalent
3. Transformer current sensor	LEM LA 55-P or equivalent

4. Secondary DC bus voltage sensor	LEM LV 25-P or equivalent
5. Output voltage sensor	LEM LV 25-P or equivalent
6. Output current sensor	LEM LA 25-P or equivalent

Heatsinks:
Primary side devices should be attached to the heat sink (OMNI-UNI-41-75, Wakefield Solutions) and be aircooled with fan (9GA0612PIK60, Sanyo Denki). Two devices should share one of these heat sinks. Similarly on the secondary side, two devices should share one heat sink (OMNI-UNI-41-75, Wakefield Solutions). The secondary side device need not be fan cooled. The heatsink temperature should not exceed 25 degree Celsius more than the ambient temperature.

DC-AC converter transformer design data:	
Frequency of operation (in Hz)	50 kHz
Tx secondary rms current (in amp)	11 A
Tx secondary peak current (in amp)	27 A
Designed Ns/Np	3
Net leakage inductance referred to sec. (in uH)	No constraint; preferably as low as can be achieved
Designed magnetization current (Primary)	No constraint up to 1.5 A (peak, primary); preferably as low as can be achieved
Magnetizing inductance (primary) (in uH)	As high as possible
Tx primary current (rms) (A)	33 A
Tx primary current peak (A)	80 A
Transformer Primary Voltage Magnitude (max)	141(nominal) V(primary); Refer to actual waveform in Fig.2; and 10% more in case of maximum
Transformer Primary Voltage Magnitude (min)	133 (nominal) V(primary); Refer to actual waveform in Fig.2; and 10% less in case of minimum

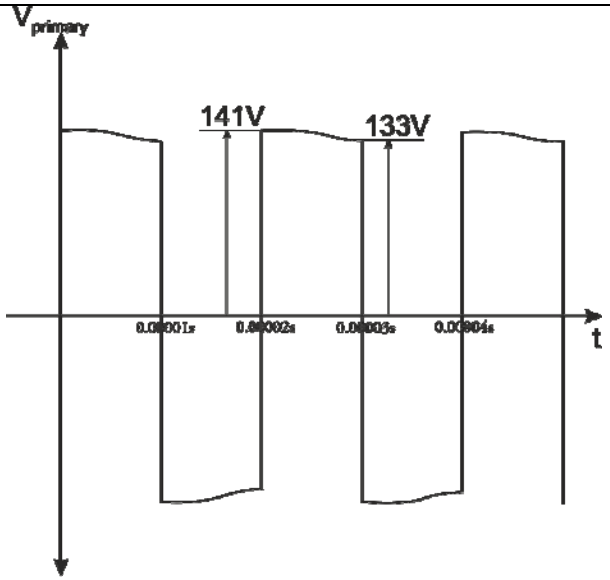


Figure 2: Transformer secondary voltage

Important: Loss in Txr: < 25W; This implies total ac resistance at 50KHz (referred to primary) $R_{(ac)}$< 27 mOhm. This corresponds to efficiency >99% expected from this design. If the designer is not sure about these values at the design stage then he should first design it as best as he can and then provide us with the measurement data. A few iterations may be required. Transformers and inductors should be clamped to a base plate.

Control signal requirments FPGA

The control board and the control logic will be designed at IIT Kharagpur and therefore that is not in the scope of deliverables. However, the space and compatible connectors for placing and mounting the control board (the dimensions and pin details are given in the figure below) will have to be provided in the main printed circuit board. This control connector with interface the switching signals for device gate drives and isolated analog feedback signals from the sensors.

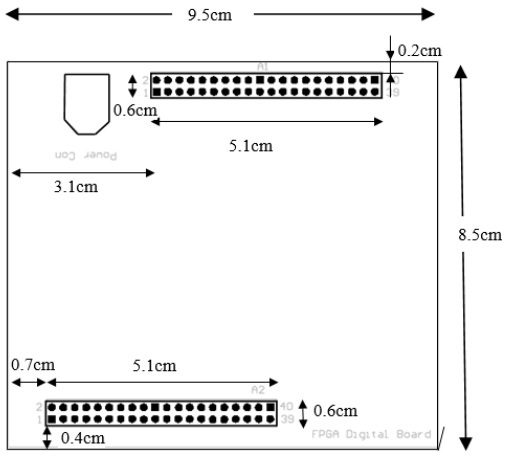
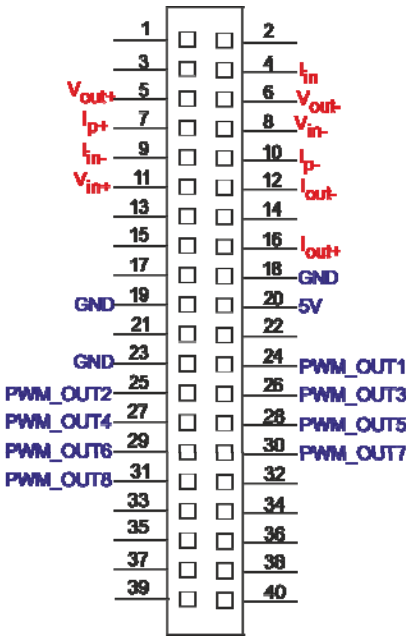
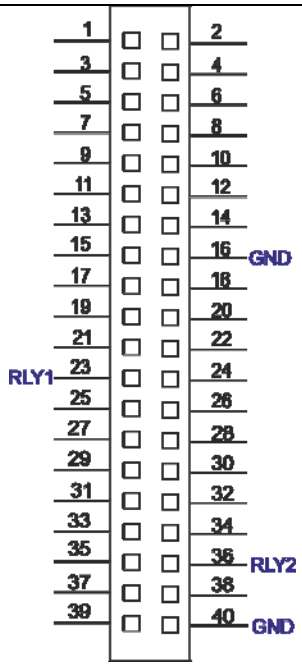


Figure 3 FPGA Board Dimensions



Connector 1



Connector 2

Fig.3. Dual row 40 pin female connector for FPGA

4. 3kW 70V DC to 400V DC CSVS DAB Converter

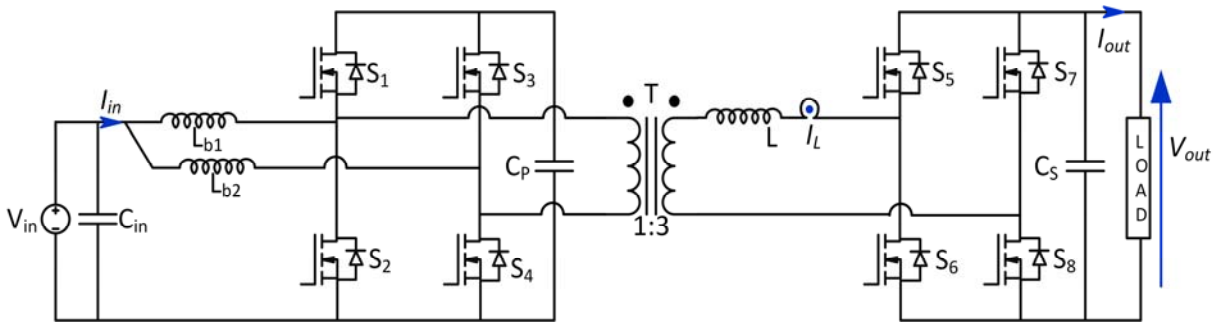


Fig. Circuit diagram of current source voltage source dual active bridge converter

Converter Specifications:

Parameter	***Value***
Rated output power	3kW
Nominal input voltage (V_{in})	70V DC
Nominal output voltage (V_{out})	400V DC
Switching frequency (f_s)	50kHz
Input Capacitance (C_{in})	20uF (2 Capacitors each of MKT 1820 *Vishay*)
Primary side mosfets (S_1,S_2,S_3,S_4)	*Infineon* IRFP4668PBF
Secondary side mosfets (S_1,S_2,S_3,S_4)	*Cree* C2M0040120D, SiC based
Primary DC bus capacitance (C_P)	20uF, 1KV (DC film capacitor Vishay MKP1848S62010JY5F)
Secondary DC bus capacitance (C_S)	20uF, 1KV (DC film capacitor Vishay MKP1848S62010JY5F)
Boost inductor (L_{b1} , L_{b2})	100uH RMS current 25A Peak current 30A Resistance at 50KHz < 20mOhm
Transformer (T)	Turns ratio 1:3 RMS current through primary 36A RMS current through secondary 12A Maximum Flux Density = 0.12T for Epcos N87Core material, 0.135T for FerroxCube 3C95 Material Magnetizing inductance (primary) (in uH) : around 200uH Power Loss < 25W so that an efficiency of 99% is obtained which implies that the total AC resistance at 50kHz referred to primary < 20mOhm. Suggestion: Generally, the winding is done using copper foils or stranded copper litz wire. Anyone of them or some better technique can be used.
Dual active bridge inductor (L)	70uH RMS current 10A Peak current 12A Resistance at 50KHz < 20mOhm

Sensors:

Sensing Signal	Sensor specification
1. Input current (I_{in})	LEM LA 25-P or equivalent
2. Output current (I_{out})	LEM LA 25-P or equivalent
3. Output Voltage (Vout)	LEM LV 25-P or equivalent
4. High frequency inductor current (I_L)	High frequency current sensor using toroid

Heatsinks:

Power semiconductor switches should be attached to the heat sink (OMNI-UNI-41-75, Wakefield Solutions). Two devices should share one of these heat sinks.
The heatsink temperature should not exceed 25 degree Celsius more than the ambient temperature.

Protections to be incorporated:

1. Over-voltage protection
2. Over current protection

Control signal requirments FPGA

The control board and the control logic will be designed at IIT Kharagpur and therefore that is not in the scope of deliverables. However, the space and compatible connectors for placing and mounting the control board (the dimensions and pin details are given in the figure below) will have to be provided in the main printed circuit board. This control connector will interface the switching signals for device gate drives and isolated analog feedback signals from the sensors.

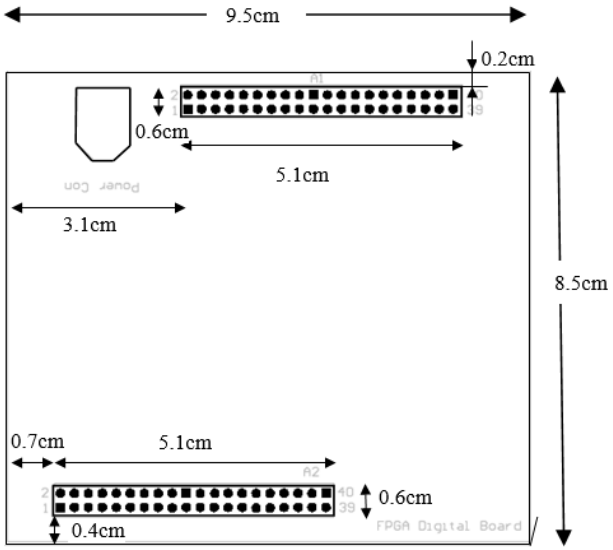


Figure 3 FPGA Board Dimensions

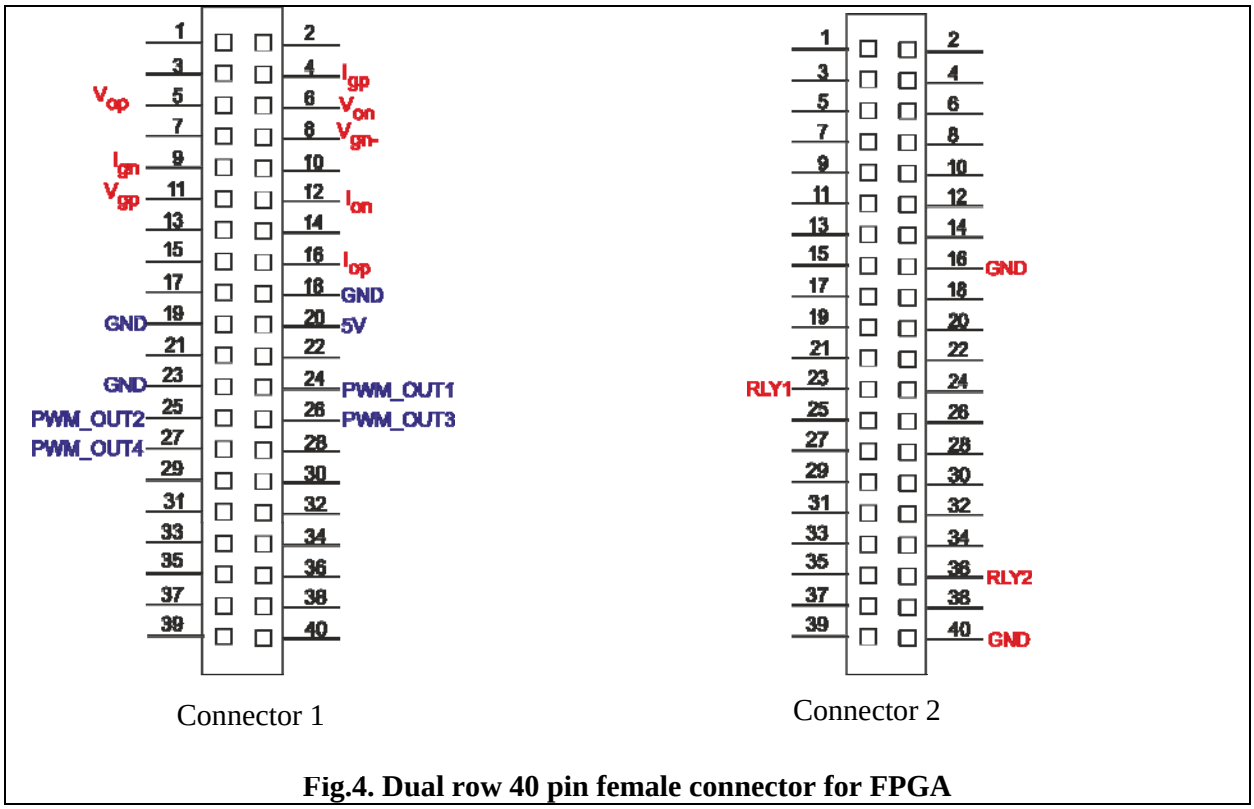


Fig.4. Dual row 40 pin female connector for FPGA

NOTE: Any deviation or modification from the above specification has to be brought to the attention of Dr. Souvik Chattopadhyay, IIT Kharagpur well in advance before implementation. A detailed discussion may be required for any such modification.

GENERAL TERMS & CONDITIONS

PLEASE SPECIFICALLY INDICATE THE FOLLOWING POINTS IN YOUR QUOTATIONS AND COMPLY THE TERMS AS MENTIONED HEREUNDER:-

1. TENDER ARE INVITED COMPLYING THE REQUIREMENT FOR TENDER AS DETAILED IN THE TENDER SPECIFICATION TO BE SUBMITTED IN THE COMPANY'S / FIRM'S LETTERHEAD NEATLY PRINTED / TYPED DULY SIGNED BY AUTHORIZED PERSON WITH THE SEAL OF THE BIDDERS. ALL ENVELOPS CONTAINING THE TENDER SHOULD BE PROPERLY SEALED. SEPARATE ENVELOPS SHOULD BE USED FOR TECHNICAL AND PRICE BID AND INDICATION TO THEIR EFFECT MAY PLEASE BE SUPERSCRIBED ON THE ENVELOP.

THE FOLLOWING DOCUMENTS ARE REQUIRED FROM THE INDIAN AGENTS OF FOREIGN FIRMS:

1.1 FOREIGN PRINCIPAL'S PROFORMA INVOICE INDICATING THE COMMISSION PAYABLE TO THE INDIAN AGENT AND NATURE OF AFTER SALES SERVICE TO BE RENDERED BY THE INDIAN AGENT.

1.2 COPY OF THE AGENCY AGREEMENT WITH THE FOREIGN PRINCIPAL INDICATING THE NATURE OF AFTER SALES SERVICES, PRECISE RELATIONSHIP BETWEEN THEM AND THEIR MUTUAL INTEREST IN THE BUSINESS.

1.3 PLEASE ENCLOSE THE DOCUMENT(S) RELATED TO THE ENLISTMENT OF THE INDIAN AGENT WITH DIRECTOR GENERAL OF SUPPLIES & DISPOSALS (DGS & R) UNDER THE COMPULSORY REGISTRATION SCHEME OF MINISTRY OF FINANCE.

2. TECHNICAL CATALOGUE/LEAFLET SHOULD BE ENCLOSED WITHOUT FAIL. PROVIDE COMPLIANCE STATEMENT WITH RESPECT TO THE TECHNICAL SPECIFICATIONS MENTIONED ABOVE.

3. PLEASE CONFIRM WHETHER YOU ARE AUTHORISED TO QUOTE ON BEHALF OF YOUR PRINCIPALS AND IF SO, PLEASE ENCLOSE A COPY OF SUCH AUTHORISATION WITH YOUR QUOTATION.

4. **PRICE BIDS FOR FOREIGN FIRMS**: PRICES ARE TO BE QUOTED ON '**EX-WORKS**' DULY PACKED OR ON **"FCA/FOB"** INTERNATIONAL PORT" BASIS AND ALSO INCLUDING AGENCY COMMISSION PAYABLE TO YOUR INDIAN AGENTS, IF ANY SHOWING CLEARLY THE FOLLOWING BREAK UP:-

   I) EX-WORKS PRICE
   II) PACKING & FORWARDING
   III) FREIGHT
   IV) ANY OTHER RELEVANT EXPENSES.
   V) TAXES PAYABLE BY THE INSTITUTE

   INSURANCE WILL BE PAID BY OUR INSTITUTE SEPARATELY AND SHOULD NOT FORM PART OF THE QUOTED PRICE.

   PRICE BIDS FOR INDIAN FIRMS: PRICES ARE TO BE QUOTED ON F.O.R., IIT KHARAGPUR, ON DOOR DELIVERY BASIS CLEARLY SHOWING THE BREAK UP.

5. **PERIOD OF VALIDITY**: BIDS SHALL REMAIN VALID FOR ACCEPTANCE FOR A PERIOD OF 120 DAYS FROM THE DATE OF OPENING.

6. INDIAN AGENTS ADDRESS AND PERCENTAGE OF AGENCY COMMISSION INCLUDED IN ABOVE F.O.B./EX-WORKS PRICE. (THIS WILL BE PAID TO THE INDIAN AGENTS IN INDIAN RUPEES ONLY AND NOT IN **FE).** PLEASE ENCLOSE COPY OF AGENCY AGREEMENT ENTERED INTO WITH YOUR

PRINCIPALS INDICATING THE NATURE OF AFTER SALES SERVICES OF INDIAN AGENTS, PRECISE RELATIONSHIP & MUTUAL INTEREST IN THE BUSINESS.

7. **MEASUREMENTS/WEIGHT:** NETT/GROSS OF THE CONSIGNMENT. IN CASE OF AN ORDER, YOU SHALL USE AIR WORTHY PACKAGE (AS APPLICABLE) DULY CERTIFIED WITH DOCUMENTS – PLYTO – SANITARY CERTIFICATE (AS PER QUARANTINE ORDER 2003).

8. **SCOPE OF SUPPLY**: SHOULD INCLUDE FREE INSTALLATION AND COMMISSIONING

9. **PAYMENT TERMS** FOR FOREIGN FIRMS

   The offer will be made on a single currency and only one PO will be issued for the entire scope of the supply.

   A) 90% PAYMENT THROUGH SIGHTDRAFT/FORIGN DEMAND DRAFT/LC (EXCEPTIONAL CASES)/SWIFT TELE TRANSFER AFTER RECEIPT OF STORE IN GOOD ORDER AND CONDITION AND 10% AFTER SUCCESSFUL INSTALLATION & COMMISSIONING.

   B) BANK CHARGES ON LC/SD (WITHIN INDIA APPLICANT ACCOUNT AND OUTSIDE INDIA TO BENEFICIARY ACCOUNT).

   PAYMENT TERMS FOR INDIAN FIRMS

   A) 100% PAYMENT THROUGH CROSSED ACCOUNT PAYEE CHEQUE / ELECTRONIC TRANSFER AFTER RECEIPT OF STORE IN GOOD ORDER & CONDITION AND SUCCESSFUL INSTALLATION & COMMISSIONING.

   B) ENSURE MENTIONING

   i) BANK DETAILS OF THE BENEFICIARY, GST NO. AND PAN NUMBER

   ii) FULL NAME AND ADDRESS OF THE BENEFICIARY ON WHOM ORDER HAS TO BE PLACED

10. WHETHER ANY EXPORT LICENCE IS REQUIRED FROM YOUR GOVERNMENT, IF SO, PLEASE CONFIRM WITH DETAILS.

11. COUNTRY OF ORIGIN OF THE GOODS IS TO BE MENTIONED.

12. THE INSTITUTE SHALL PROVIDE THE CONCESSIONAL CUSTOMS DUTY AND EXCISE DUTY EXEMPTION CERTIFICATE AS PER GOVT. NOTIFICATION NO. 51/96 CUSTOMS DATED: 23.07.1996 AND CENTRAL EXCISE DUTY EXCEMPTION IN TERMS OF GOVT. NOTOFICATION NO. 10/97 – CENTRAL EXCISE DATED: 01.03.1997 AS AMENDED FROM TIME TO TIME.

13. **LIQUIDATED DAMAGES**: THE STORES SHOULD BE DELIVERED / DISPATCHED TO DESTINATION AND READY FOR OPERATION NOT LATER THAN THE DELIVERY DATE SPECIFIED. IT THE SUPPLIER FAILS TO DELIVER ANY OR ALL THE STORES OR PERFORM THE SERVICE BY THE SPECIFIED DATE, LIQUIDATED DAMAGES AT 1% PER MONTH OR PART THEREOF IN RESPECT OF THE VALUE OF STORES WILL BE DEDUCTED FROM THE CONTRACT PRICE SUBJECT TO A MAXIMUM OF 5%. ALTERNATIVELY, THE ORDER WILL BE CANCELLED AND THE UNDELIVERED STORES PURCHASED FROM ELSEWHERE AT THE RISK AND EXPENSE OF SUPPLIER.

14. **PATENT RIGHTS**: THE SUPPLIER SHALL INDEMNIFY THE PURCHASE AGAINST ALL THIRD PARTY CLAIMS OF INFRINGEMENT OF PATENT, TRADEMARK OR INDUSTRIAL DESIGN RIGHTS ARISING FROM USE OF THE GOODS OR ANY PART THEREOF IN INDIA.

15. ONLY THOSE BIDDERS WHO'S BIDS HAVE BEEN TECHNICALLY FOUND ACCEPTABLE WILL ONLY BE INVITED FOR PARTICIPATION IN THE PRICE BID.

16. THOSE BIDDERS WHO DO NOT RECEIVE ANY COMMUNICATION FOR PARTICIPATION IN PRICE BID OPENING MEETING MAY PRESUME THAT THEIR BID HAS NOT BEEN ACCEPTED BY THE INSTITUTE.
17. CONDITIONAL OFFER WILL NOT BE ACCEPTED.

18. LATE TENDERS I.E. TENDER RECEIVED AFTER THE DUE DATE AND TIME OF SUBMISSION AS MENTIONED ABOVE SHALL NOT BE ACCEPTED.

19. BIDDERS TO ENCLOSE THE FOLLOWING DOCUMENTS:-

    A) INCOME TAX RETURN (3 YRS) AND LATEST SALES TAX RETURN (GST No.), AND PAN NO.

    B) BANKER'S SOLVENCY CERTIFICATE

    C) SUMMARY OF AUDITED STATEMENT OF ACCOUNTS FOR THE LAST THREE YEARS TO BE ENCLOSED AND FINANCIAL HIGHLIGHTS AND THE KEY PERFORMANCE DURING THE LAST THREE QUARTERS TO BE ENCLOSED AS PER FORMAT:-

COMPANY'S KEY PERFORMANCE

DESCRIPTION	JAN. TO MARCH	APRIL TO JUNE	JULY TO SEPT.
GROSS REVENUE			
PROFIT BEFORE TAX			
PROFIT AFTER TAX			
RETURN ON INVESTED			
CAPITAL (ROIC)			

D) CUSTOMER SATISFACTION CERTIFICATE FROM ONE SUCH ORGANIZATION IS TO BE ATTACHED WITH THE TECHNICAL BID AND PRICE BID.

E) NAME AND ADDRESS OF MINIMUM THREE CLIENTS TO WHOM SUCH EQUIPMENT HAVE BEEN SUPPLIED SHOULD BE MENTIONED.

20. **WARRANTY / GUARANTEE**: THIS COMPREHENSIVE WARRANTY / GUARANTEE SHALL REMAIN VALID FOR **36 MONTHS** AFTER THE GOODS (OR ANY PORTION THEREOF AS THE CASE MAY BE) HAVE BEEN DELIVERED AND COMMISSIONED TO THE FINAL DESTINATION.

21. THE INSTITUTE DOES NOT BIND ITSELF TO OFFER ANY EXPLANATION TO THOSE BIDDERS WHO'S TECHNICAL BID HAS NOT BEEN FOUND ACCEPTABLE BY THE EVALUATION COMMITTEE OF THE INSTITUTE.

22. ALL TENDERS (UNLESS OTHERWISE SPECIFIED) ARE TO BE SUBMITTED / HANDED OVER TO **DR. SOUVIK CHATTOPADHYAY, DEPARTMENT OF ELECTRICAL ENGINEERING, INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR - 721 302** AND ACKNOWLEDGEMENT TO BE OBTAINED.

IMPORTANT

1. IIT Kharagpur authority may accept or reject any or all the bids in part or in full without assigning any reason and does not bind itself to accept the lowest bid. The Institute at its discretion may change the quantity / upgrade the criteria / drop any item or part thereof at any time before placing the Purchase Order.

2. Promptly make arrangements for repair and / or replacement of any damaged item (s) irrespective of settlement of claim.

3. In case of any dispute, the decision of the Institute authority shall be final and binding on the bidders.

4. For any query pertaining to this bid document correspondence may be addressed to **Dr. Souvik Chattopadhyay**, at the address mentioned above.

LAST DATE FOR SUBMISSION OF SEALED BIDS: 31.01.2019

1) Please Note that the Institute remains closed during Saturdays & Sundays and all specified government holidays.

2) Fax, e-mail Tender will not be accepted.

3) The General Terms and Conditions as stated above relate to supply of stores / equipment /assets etc. and for specific service other terms and conditions of the Institute will apply.
